REMARKS

Claims 1-25 were pending in the application prior to this Amendment.

The Examiner allows claim 18. The Examiner indicates allowable claims 7 and 14 if rewritten in independent form to include the limitation of the base and any intervening claims.

The Examiner rejects claims 1-4, 9-12, 15, 17 and 19 under 35 U.S.C. § 102(e) as being anticipated by Kim (U.S. 6,219,023). The Examiner rejects claims 5, 13, 16, and 22 under 35 U.S.C. § 103(a) as being unpatentable over Kim in view of Choi et al (U.S. 5,742,349). The Examiner rejects claims 6 and 8 under 35 U.S.C. § 103(a) as being unpatentable over Kim in view of Faroudja et al (U.S. 6,222,589). The Examiner rejects claims 20-21 and 23-25 under 35 U.S.C. § 103(a) as being unpatentable over Kim in view of Imaizumi et al (U.S. 2002/0158868).

The applicants amend claims 2-8, 10-15, 16-17, and 21-25 and add claim 26.

The application remains with claims 1-26 after entering this Amendment.

The applicants add no new matter and request reconsideration.

Claim Objections

The applicants thank the Examiner for allowing claim 18 and indicating allowable claims 7 and 14. The applicants rewrite claims 16 and 17 to depend from claim 18.

The applicants rewrite claims 7 and 14 in independent form to include all the limitations of base claims and any intervening claims. The applicants amend claims 2-6 and 8 to depend from allowable claim 7.

The applicants add claim 26 to include limitations indicated as allowable by the Examiner. The applicants agree that Kim, Choi, Faroudja, Imaiizumi or their combination disclose the invention recited in claim 26.

Claims 2-8, 10-13, 14, 16-18, and 26 are in condition for allowance.

Claim Rejections Under § § 102 and 103

The Examiner alleges Kim discloses all of the limitations of independent claims 1, 9, 15, and 19. The applicants disagree for the reasons that follow.

Claim 1 recites *a failsafe enable circuit to generate a failsafe enable signal responsive to the input vertical refresh rate*. Claims 9 and 19 include similar limitations. The Examiner alleges the failsafe enable circuit recited is disclosed by Kim's output control logic circuit 650 comprising inverters 651 and 652 because "the two inverters 651 and

651...enable the read enable signals LMRE1 and LMRE2." The Examiner points to Figure 7, 12, and column 8, lines 39-41. But the output control circuit 650 does not generate the read enable signals LMRE1 and LMRE2 as is clearly shown in Figures 3 and 7. In Figure 3, the read enable signals LMRE1 and LMRE2 are shown as generated by the memory operation control block 610 and provided to the output control logic circuit 650 as inputs. Figure 7 shows the read enable signals as inputs to the inverters 651 and 652.

Kim explains that the "output control logic circuit 650 is constituted by two inverters 651 and 652 which enable the read enable signals LMRE2 and LMRE1 of the most significant two bits from the memory operation control circuit 610 to be inverted." That is, the output control logic 650 inverts the most significant two bits from the memory operation control circuit 610, and not that the circuit 650 generates or otherwise creates the read enable signals LMRE1 and LMRE2. The output control logic circuit 650 generates the output selection signals SO0 and SO1 responsive to the read enable signals LMRE1 an LMRE2, respectively. "Each of the multiplexers 420a, 420b and 420c outputs one of the outputs of the line memories LM0, LM1 and LM2 of each memory block in response to the output selection signals SO0 and SO1 from, the output control logic circuit 650." Kim Figures 3, 7, and column 8, lines 39-47.

Thus, the output control logic circuit 650 cannot disclose the failsafe enable circuit because 1) it does not generate a failsafe enable signal at all; and 2) it does not generate a failsafe enable signal responsive to the input vertical refresh rate. That is, even if the Examiner alleged the output selection signals SO0 and SO1 to be the failsafe enable signals, these output selection signals are not generated by the output control logic circuit 650 responsive to the input vertical refresh rate. Rather, the circuit 650 generates the output selection signals SO0 and SO1 by inverting the read enable signals LMRE1 and LMRE2, respectively.

Contrary to the Examiner's allegations, it is the read operation control circuit 610 that generates the read enable signals LMRE1 and LMRE2. "The read operation control circuit 610 generates read enable signals LMRE0-LMRE2 corresponding to each line memory in response to the read pixel clock signal R_Dclk from the clock generator 200 and the memory index signals WLM0 and WLM1." Kim, column 9, lines 9-13. This portion of the specification is consistent with the block diagrams of Figures 3 and 7.

The read operation control circuit 610, however, does not operate responsive to any input vertical refresh rate. The read operation control circuit 610 operates responsive to the read pixel clock signal R_Dclk as clearly shown in Figure 14 and explained at column 12,

lines 3-6 ("The flip-flops 735a-735c are enabled by the read pixel clock signal R_Dclk to generate the read enable signals LMRE0, LMRE1, and LMRE2, respectively.").

Claim 1 recites *a failsafe circuit to generate an internal vertical refresh rate responsive to the failsafe enable signal, the internal vertical refresh rate being a predetermined fraction of the input vertical refresh rate.* Claims 9 and 19 include similar limitations. The Examiner fails to identify which of Kim's signals he believes discloses the failsafe vertical refresh rate recited other than to indicate that Table 1 shows "a ratio resolution before and after conversion, and color signal RGB corresponding to 5 lines are change into color signals 8 lines, see column 5, lines 18-23. The applicants do not understand the Examiner's rejection since, as we point out in the previously submitted Amendment, Kim clearly indicates that it maintains constant the frequency of the vertical synchronization signal Vsync.

Kim discloses at column 4, lines 59-61:

"With the apparatus, **the frequency of the vertical synchronization signal Vsync is kept constant...**"

Kim discloses at column 5, lines 24-30:

"Next, if the SVGA mode signals are fed to the LCD controller (i.e., the video signal converter) according to this embodiment, **the frequency of the vertical synchronization signal Vsync is kept constant...**"

Table 1 discloses a system in which the vertical refresh signal Vsync is kept constant while the horizontal refresh signal Hsync and the dot clock Dclk are increased relative to the input frequency. Again, the vertical refresh signal does not change.

Claim 15 recites *a flip-flop to generate a first signal responsive to an input vertical refresh rate.* The Examiner alleges Kim's flip-flops 725a-725c disclose the recited flip-flop. But Kim's flip-flops 725a-725c do not operate responsive to an input vertical refresh rate as recited.

Claim 15 recites *an inverter to invert the first signal.* The Examiner alleges inverters 723a-723d invert the recited first signal. But if Kim's flip-flops 725a-725c disclose the recited flip-flop —we do not believe they do as we explain above—, the first signal then is necessarily one of line memory write enable signals LMWE0-2. None of the inverters 723a-723d invert any of signals LMWE0-2.

Claim 15 recites *a logic gate to generate an internal vertical refresh rate by logically manipulating the first signal and the input vertical refresh rate, the internal vertical refresh rate being a factor of the input vertical refresh rate.* The Examiner alleges logic gates 724a-

724c disclose the recited logic gate, then they must generate the recited internal vertical refresh rate. Nothing in Kim's specification nor in Figures 10, 12, or 16 indicate that logic gates 724a-c generate an internal vertical refresh rate but rather provide the D input to flip-flops 725a-c. The Examiner asks the applicants to "see Figure 12" for an identification of the internal vertical refresh rate. None is found by the applicants.

Finally, claim 15 recites *a multiplexer to select the internal vertical refresh rate responsive to the enable signal.* The Examiner argues multiplexers 631-633 disclose the multiplexer recited. But it is unclear how the multiplexers 631-633 are connected to the circuit in Figure 12 that the Examiner uses as a basis for disclosing the rest of the elements recited in the claim. The multiplexers 63-633 do not select between any signal associated with or otherwise generated (or that exist for that matter) by the circuit in Figure 12.

Conclusion

The applicants request reconsideration and allowance of all claims. The applicants encourage the Examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (703) 872-9306 on March 25, 2005.

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